UG-2832HLBEG04

UG-2832HLBEG05

UG-2832HSWEG04

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Evaluation Kit User Guide

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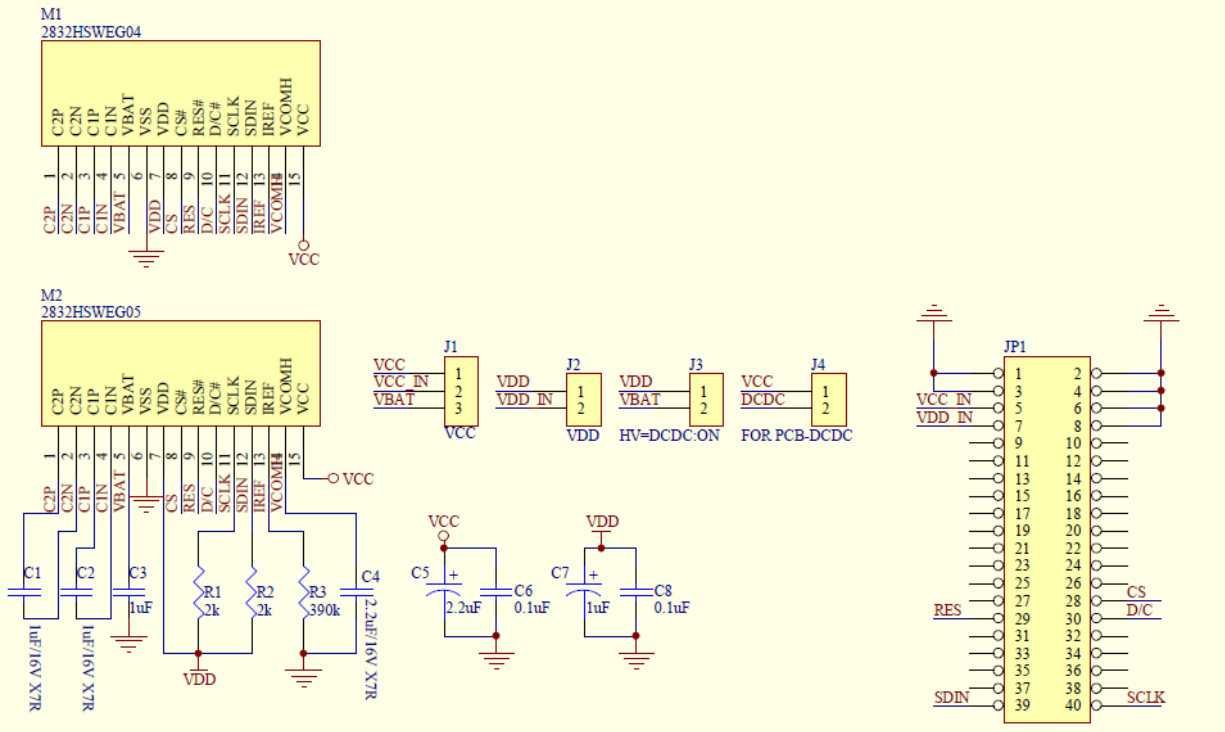
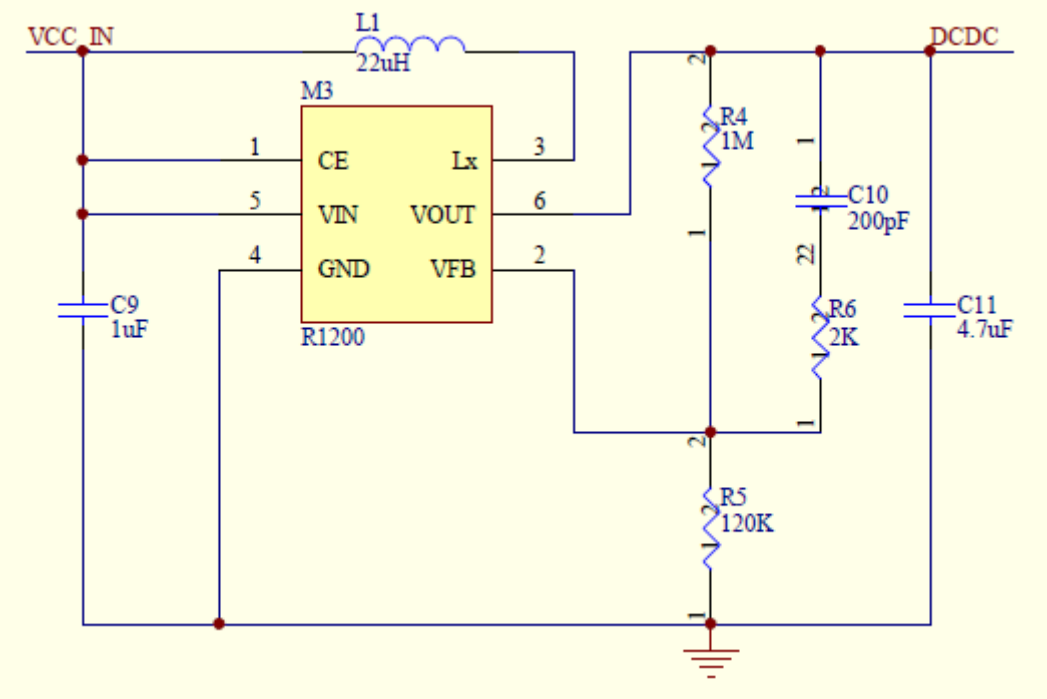
1. REVISION HISTORY

Date	Page	Contents	Version
2011/12/05		Preliminary	Preliminary 0.0

2. EVK Schematic





3. Symbol define

3.1 JP1：

D0~D1：When serial interface mode is selected, D0(SCLK) will be the serial clock input,D1(SDIN) will be the serial data input,

D/C：This is DATA/COMMAND control pin. When it is Pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register.

RES：This pin is reset signal input(active LOW).

CS：This pin is chip select input(active LOW).

VCC_IN：Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.

VDD_IN：Low voltage power supply

GND：Power supply ground.

3.2 Jump

J1-VCC：Selects VCC_IN voltage or DC-DC output voltage.

J2-VDD：jump link VDD_IN pin and VDD pin.

J3-HV=DCDC:ON：charge pump disable

J4-FOR PCB-DCDC：DC-DC Chip FOR R1200

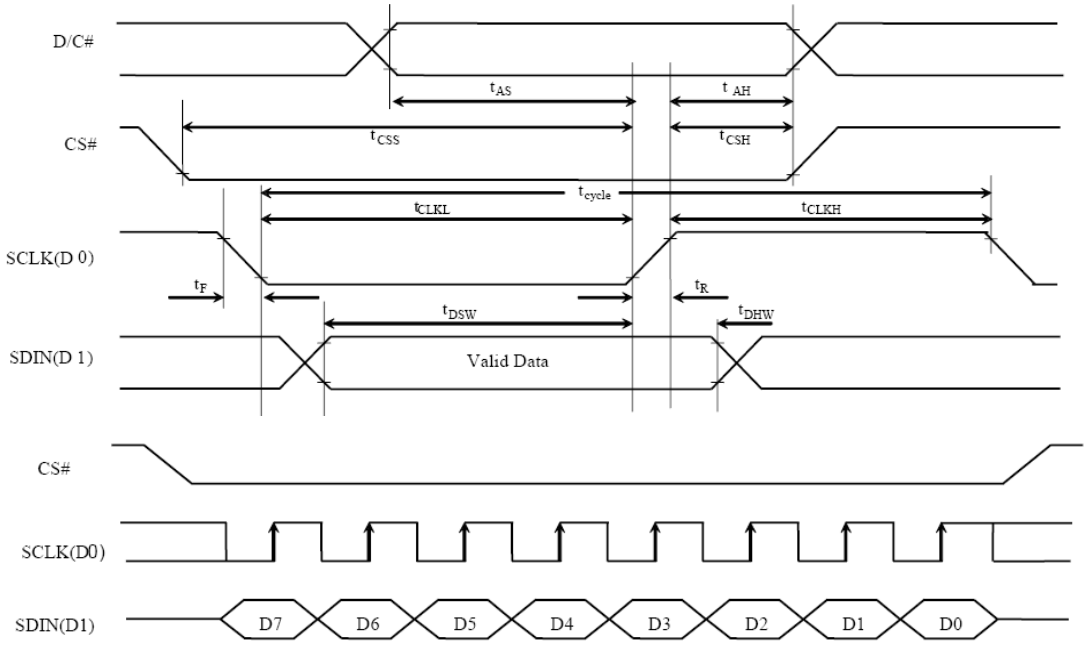
4.TIMMING CHARACTERISTICS

4-wire Serial Interface Timing Characteristics:

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

4-wire Serial Interface Characteristics



5.EVK use introduction

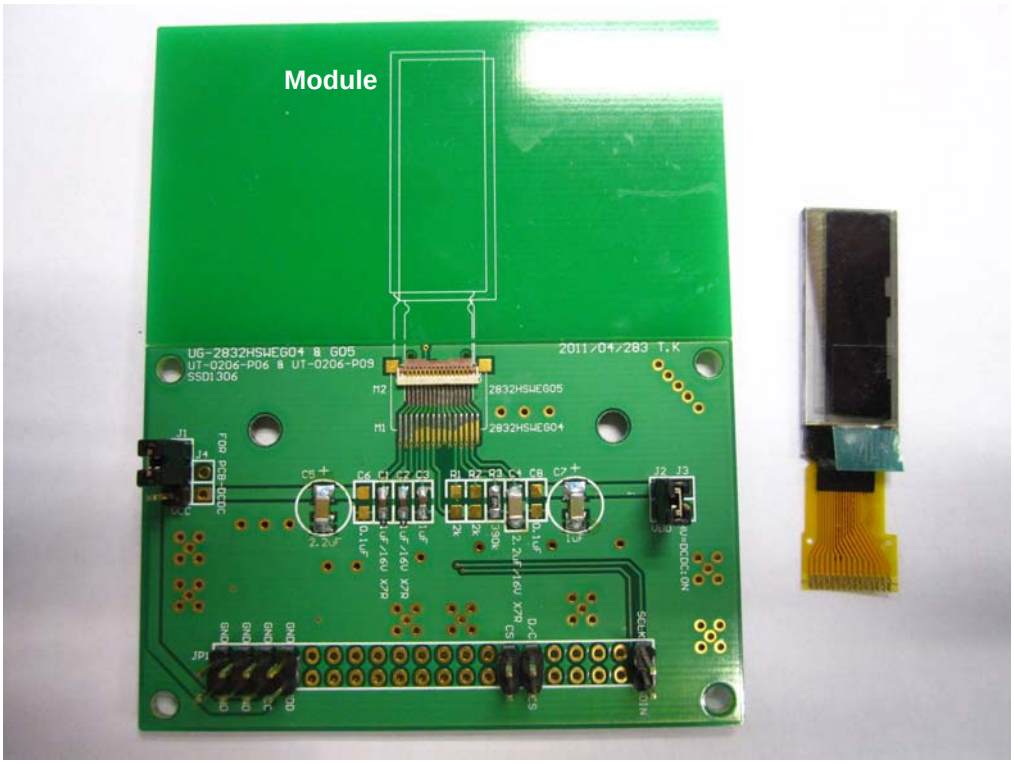


Figure 1 EVK PCB and OLED Module

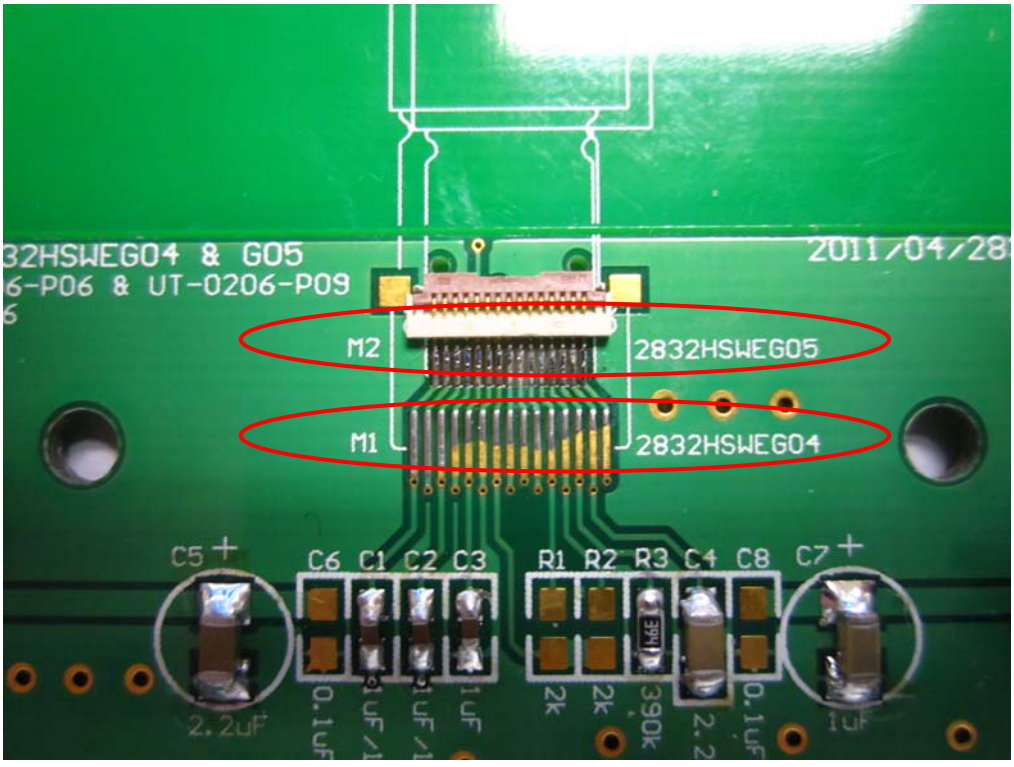


Figure 2 The combination of the module and EVK

M1 for UG-2832HSWEG04

M2 for UG-2832HSWEG05

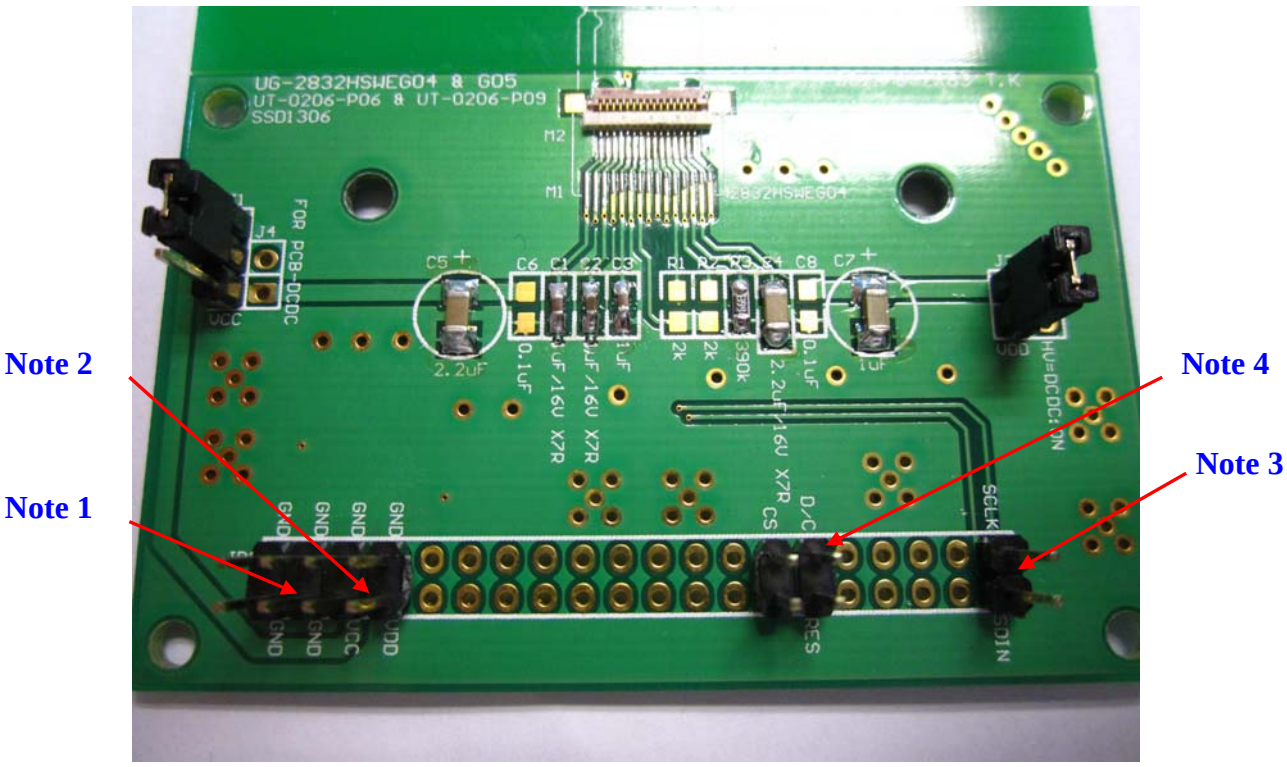


Figure 3 EVK with test platform

Note 1：It is logic voltage supply.

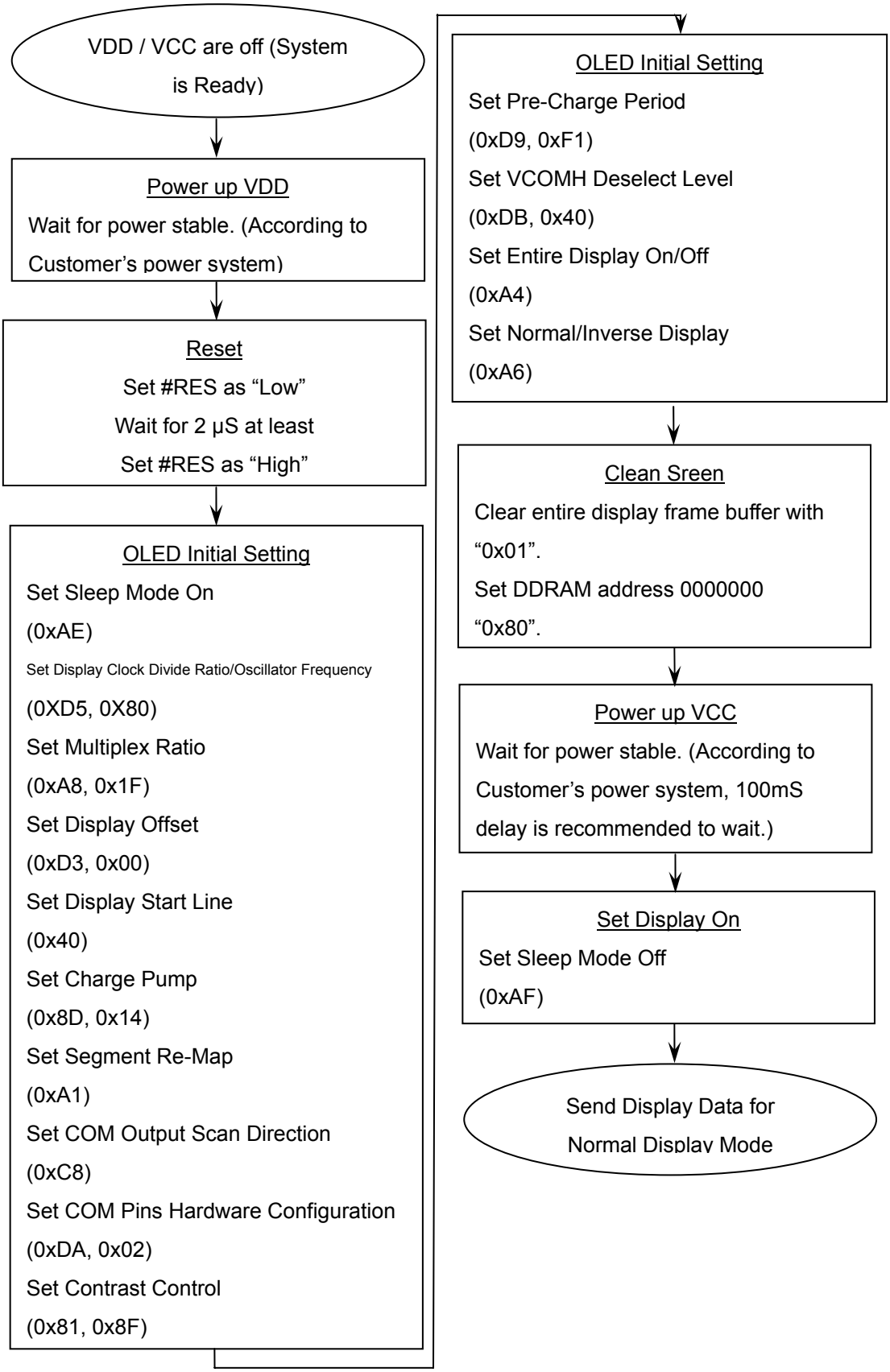
Note 2：It is OLED high voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin SCLK / SDIN.(D0-D1)

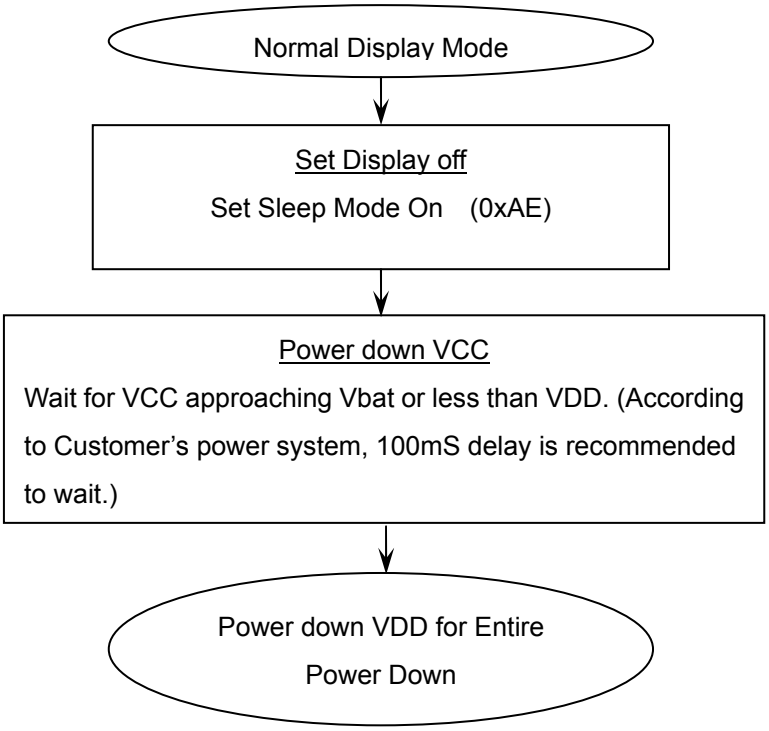
Note 4：Those are leading wire connect to control board. Those are control pin. (D/C, CS, RES)

6. Reference sequence

6.1 Power on sequence:

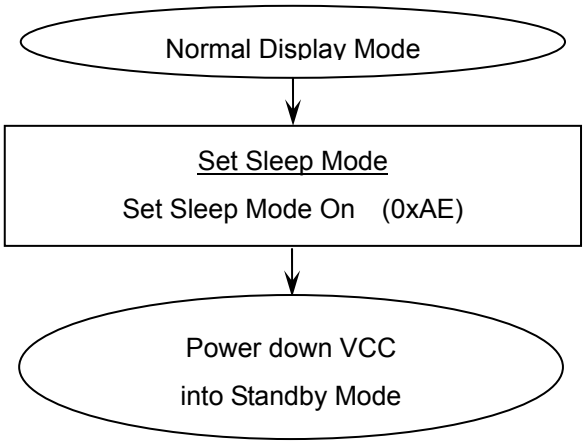


6.2 Power down sequence:

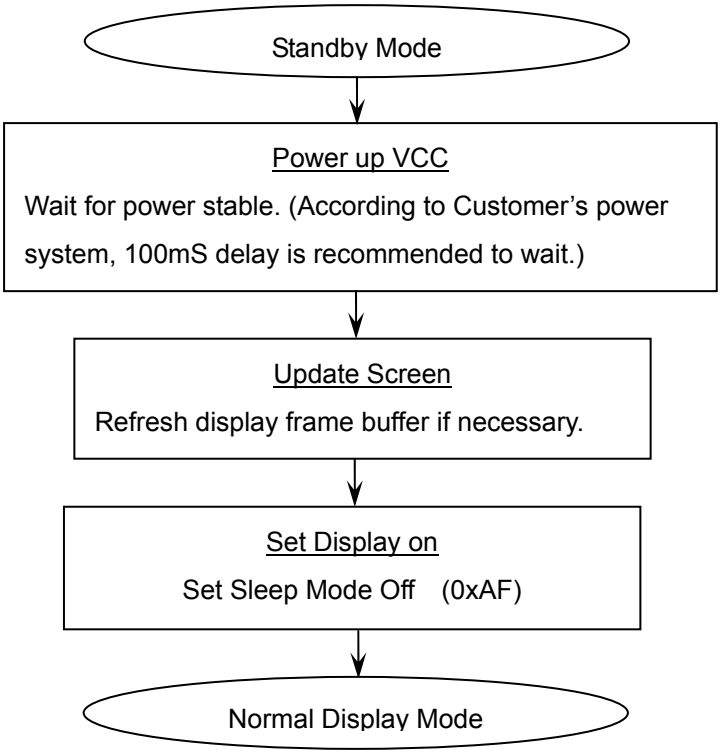

Normal Display Mode
Set Display off
Set Sleep Mode On (0xAE)
Power down VCC
Wait for VCC approaching Vbat or less than VDD. (According to Customer's power system, 100mS delay is recommended to wait.)
Power down VDD for Entire Power Down

Note: VDD should not be Power OFF before VCC Power OFF.

6.3 Standby sequence:



6.4 Wake up sequence:


Standby Mode
Power up VCC
Wait for power stable. (According to Customer's power system, 100mS delay is recommended to wait.)
Update Screen
Refresh display frame buffer if necessary.
Set Display on
Set Sleep Mode Off (0xAF)
Normal Display Mode